100Gb/s CFP Optical Transceiver

Features

-
-
-
-
-
-
-
-
-

Standards

Note1. The supply current includes CFP module's supply current and test board working current.
Note2. Average launch power ,each lane(min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance
Note3. Even if the TDP<1dB, the OMA(min) must exceed this value
Note4. Transmitter reflectance is defined looking into the transmitter
Note5. The receiver shall be able to tolerate , without damage, continuous exposure to an optical input signal having this average power level
Note6.

					Vendor Datasheet
Hardware MOD_LOPWR deassert	t_MOD_LOPWR_deassert			ms	Value is dependent upon module start-up time.Please See register"Maximum High-Power-up ime"in "CFP MSA Management Interface Specification"
Receiver Loss of Signal Assert Time	t_loss_assert		100	us	Maximum value designed to support telecom applications
Receiver Loss of Signal De-Assert Time	t_loss_deassert		100	us	Maximum value designed to support telecom applications
Global Alarm Assert Delay Time	GLB_ALRMn_assert		150	ms	This is a logical "OR" of Associated MDIO alarm& status registers.Please see MDIO document for further details
Global Alarm De-assert Delay Time	GLB_ALRMn_deassert		150	ms	

High Speed Electrical Characteristics

Reference Clock Characteristics

		Min	Typ	Max	Unit	Notes
Impedance	Zd	80	100	120	Ω	
Frequency			161.1328125/644.53125		MHz	1/64 or 1/16 of electrical lane rate
Frequency Stability	△f	-100		100	ppm	For Ethernet applications
		-20		20		For Telecom applications
Output Differential Voltage	V_{DIFF}	400		1200	mV	Peak to Peak Differential
RMS jitter[1,2]	σ			10	ps	Random Jitter Over frequency band of 10KHz<f<10MHz
Clock Duty Cycle		40		60	%	
Clock Rise/Fall Time 10%/90%	$t_{r/f}$	200		1250	ps	1/64 of electrical lane rate
		50		315		1/16 of electrical lane rate

Note1: The term “40GBASE_FR” is the 40GbE serial optical interface in the task force phase at IEEE-SA at the time of this publication. Also, 1/16 of optical lane clock is recommended for TX_MCLK and RX_MCLK

Note2: Multi-protocol modules are recommended to adopt the clock rate rate used in Telecom applications

Optional Transmitter and Receiver Monitor Clock Chara7 (o) (c) 4 (k) 3 ( ) (i) 7 (s) 4 (t) 5 (i)

8900	8EFF	RO	12x128	N/A	Reserved by CFP MSA
8F00	8FFF	N/A	2x128	N/A	Reserved for User private use
9000	9FFF	RO	4096	N/A	Reserved for vendor private use
A000	A07F	R/W	128	16	CFP Module VR1. CFP Module level control and DDM registers
A080	A0FF	RO	128	16	Reserved by CFP MSA
A100	A1FF	RO	2x128	N/A	Reserved by CFP MSA
A200	A27F	R/W	128	16	etwork Lane VR 1.Network lane specific register
A280	A2FF	R/W	128	16	Network Lane VR 2.Network lane specific register
A300	A3FF	RO	2x128	N/A	Reserved by CFP MSA

A400

801C	1	RO			
801D	1				
801E	1				
801F					
80			emp		
			Number		
			ial Number		
			ta Code		
			Lot Code		
			CLEI Code		
			A hardware Specification Revision Number		

808C 808E	2	RO	7~0	VCC Low Warning Threshold		

CFP NVR3

Network Lane BOL Measurement Registers

Hex Addr	Size	Access Type	Bit	Register Name	Content (HEX)	LSB Unit

		RW	7~0	Alarm Source Code		

A00B

			10	Lane 10 Di2 Tc 7able		
			9	Lane 9 Di2 Tc 7able		
			8	Lane 8 Di2 Tc 7able		
			7	Lane 7 Di2 Tc 7able		
			6	Lane 6 Di2 Tc 7able		
			5	Lane 5 Di2 Tc 7able		
			4	Lane 4 Di2 Tc 7able		
			3	Lane 3 Di2 Tc 7able		
			2	Lane 2 Di2 Tc 7able		
			1	Lane 1 Di2 Tc 7able		
			0	Lane 0 Di2 Tc 7able		
A014	1			**Ho2 Tc 72 Tc t Lane Co**		
		RO	15	Reserved		
		RW	14	TX PRBS Checker Enable		
		RW	13	TX PRBS Pattern 1		
		RW	12	TX PRBS Pattern 0		
		RO	11	Reserved		
		RW	10			

			13	Lane 13 Alarm and Warning Summary		
			12	Lane 12 Alarm and Warning Summary		
			11	Lane 11 Alarm and Warning Summary		
			10	Lane 10 Alarm and Warning Summary		
			9	Lane 9 Alarm and Warning Summary		
			8	Lane 8 Alarm and Warning Summary		
			7	Lane 7 Alarm and Warning Summary		
			6	Lane 6 Alarm and Warning Summary		
			5	Lane 5 Alarm and Warning Summary		
			4	Lane 4 Alarm and Warning Summary		
			3	Lane 3 Alarm and Warning Summary		
			2	Lane 2 Alarm and Warning Summary		
			1	Lane 1 Alarm and Warning Summary		
			0	Lane 0 Alarm and Warning Summary		
A01A	1	RO		**Network Lane Fault and Status Summary**		
			15	Lane 15 Fault and Status Summary		

A01B	1	RO		**Host Lane Fault and Status Summary**		
			15	Lane 15 Fault and Status Summary		
			14	Lane 14 Fault and Status Summary		
			13	Lane 13 Fault and Status Summary		
			12	Lane 12 Fault and Status Summary		
			11	Lane 11 Fault and Status Summary		
			10	Lane 10 Fault and Status Summary		
			9	Lane 9 Fault and Status Summary		
			8	Lane 8 Fault and Status Summary		
			7	Lane 7 Fault and Status Summary		
			6	Lane 6 Fault and Status Summary		
			5	Lane 5 Fault and Status Summary		
			4	Lane 4 Fault and Status Summary		
			3	Lane 3 Fault and Status Summary		
			2	Lane 2 Fault and Status Summary		
			1	Lane 1 Fault and Status Summary		
			0	Lane 0 Fault and Status Summary		
A01C	1	RO		Reserved		
Module FAWS Registers						
A01D	1	RO		**Module General Status**		
			15	Reserved		
			14	Reserved		
			13	HW_Interlock		
			12~11	Reserved		
			10	Loss of REFCLK Input		
			9	TX_JITTER_PLL_LOL		
			8	TX_CMU_LOL		
			7	TX_LOSF		
			6	TX_HOST_LOL		
			5			

A01F	1	RO		**Module Alarms and Warnings 1**		
			15~12	Reserved		
			11	Mod Temp High Alarm		
			10	Mod Temp High Warning		
			9	Mod Temp Low Warning		
			8	Mod Temp Low Alarm		
			7	Mod Vcc High Alarm		
			6	Mod Vcc High Warning		
			5	Mod Vcc Low Warning		
			4	Mod Vcc Low Alarm		
			3	Mod SOA Bias High Alarm		
			2	Mod SOA Bias High Warning		
			1	Mod SOA Bias Low Warning		
			0	Mod SOA Bias Low Alarm		
A020	1	RO		**Module Alarms and Warnings 2**		
			15~8	Reserved		
			7	Mod Aux 1 High Alarm		
			6	Mod Aux 1 High Warning		
			5	Mod Aux 1 Low Warning		
			4	Mod Aux 1 Low Alarm		
			3	Mod Aux 2 High Alarm		
			2	Mod Aux 2 High Warning		
			1	Mod Aux 2 Low Warning		
			0	Mod Aux 2 Low Alarm		
A021	1	RO		Reserved		

		RO	0	Reserved		
A025	1			**Module Alarms and Warnings 1 Latch**		
		RO	15~12	Reserved		
		RO/LH/COR	11	Mod Temp High Alarm Latch		
		RO/LH/COR	10	Mod Temp High Warning Latch		
		RO/LH/COR	9	Mod Temp Low Warning Latch		
		RO/LH/COR	8	Mod Temp Low Alarm Latch		
		RO/LH/COR	7	Mod Vcc High Alarm Latch		
		RO/LH/COR	6	Mod Vcc High Warning Latch		
		RO/LH/COR	5	Mod Vcc Low Warning Latch		
		RO/LH/COR	4	Mod Vcc Low Alarm Latch		
		RO/LH/COR	3	Mod SOA Bias High Alarm Latch		
		RO/LH/COR	2	Mod SOA Bias High Warning Latch		
		RO/LH/COR	1	Mod SOA Bias Low Warning Latch		
		RO/LH/COR	0	Mod SOA Bias Low Alarm Latch		
A026	1			**Module Alarms and Warnings 2 latch**		
		RO	15~8	Reserved		

		RW	5	RX_LOS Enable		
		RW	4	RX_NETWORK_LOL Enable		
		RW	3	Out of Alignment Enable		
		RO	2~0	Reserved		
A02A	1			**Module Fault Status Enable**		

A033 1

A220	16	RO/LH/COR		**Network Lane n Alarm and Warning Latch**		
			15	Bias High Alarm Latch		
			14	Bias High Warning Latch		
			13	Bias Low Warning Latch		
			12	Bias Low Alarm Latch		
			11	TX Power High Alarm Latch		
			10	TX Power High Warning Latch		

				Alarm Enable		
			3	RX Power High Alarm Enable		
			2	RX Power High Warning Enable		
			1	RX Power Low Warning Enable		
			0	RX Power Low Alarm Enable		
A250	16			**Network Lane n Fault and Status Enable**		
		RW	15	Lane TEC Fault Enable		
		RW	14	Lane Wavelength Unlocked Fault Enable		
		RW	13	Lane APD Power Supply Fault Enable		
		RO	12~8			

Host Lane VR1

Host Lane VR1						
Hex Addr	Size	Access Type	Bit	Register Name	Content (HEX)	LSB Unit
Host Lane FAWS Status Registers						
A400	16					

	Name				Name		
148	GND	1	3.3V_GND	111	GND	38	MOD_ABS
147	REFCLKn	2	3.3V_GND	110	N.C	39	MOD_RSTn
146	REFCLKp						

PIN#

32	PRG_CNTL3	I	LVCMOS w/PUR	Programmable Control 2 set over MDIO. MSA Default: Hardware Interlock MSB, “00”"8W, “01” "16W, “10” "24W, “11” or NC"24W=not used
33	PRG_ALRM1	O	LVCMOS	Programmable Alarm 1 set over MDIO, MSA Default: HIPWR_ON.”1”:module power up completed,”0”: module not high powered up
34	PRG_ALRM2	O	LVCMOS	Programmable Alarm 2 set over MDIO, MSA Default: MOD_READY, “1”: Ready, “0”: not Ready
35	PRG_ALRM3	O	LVCMOS	Programmable Alarm 3 set over MDIO, MSA Default: MOD_FAULT, fault detected, “1”: Fault, “0”: No Fault
36	TX_DIS	I	LVCMOS w/PUR	Transmitter Disable for all lanes, “1” or NC=transmitter disabled,”0”=transmitter enabled
37	MOD_LOPWR	I	LVCMOS w/PUR	

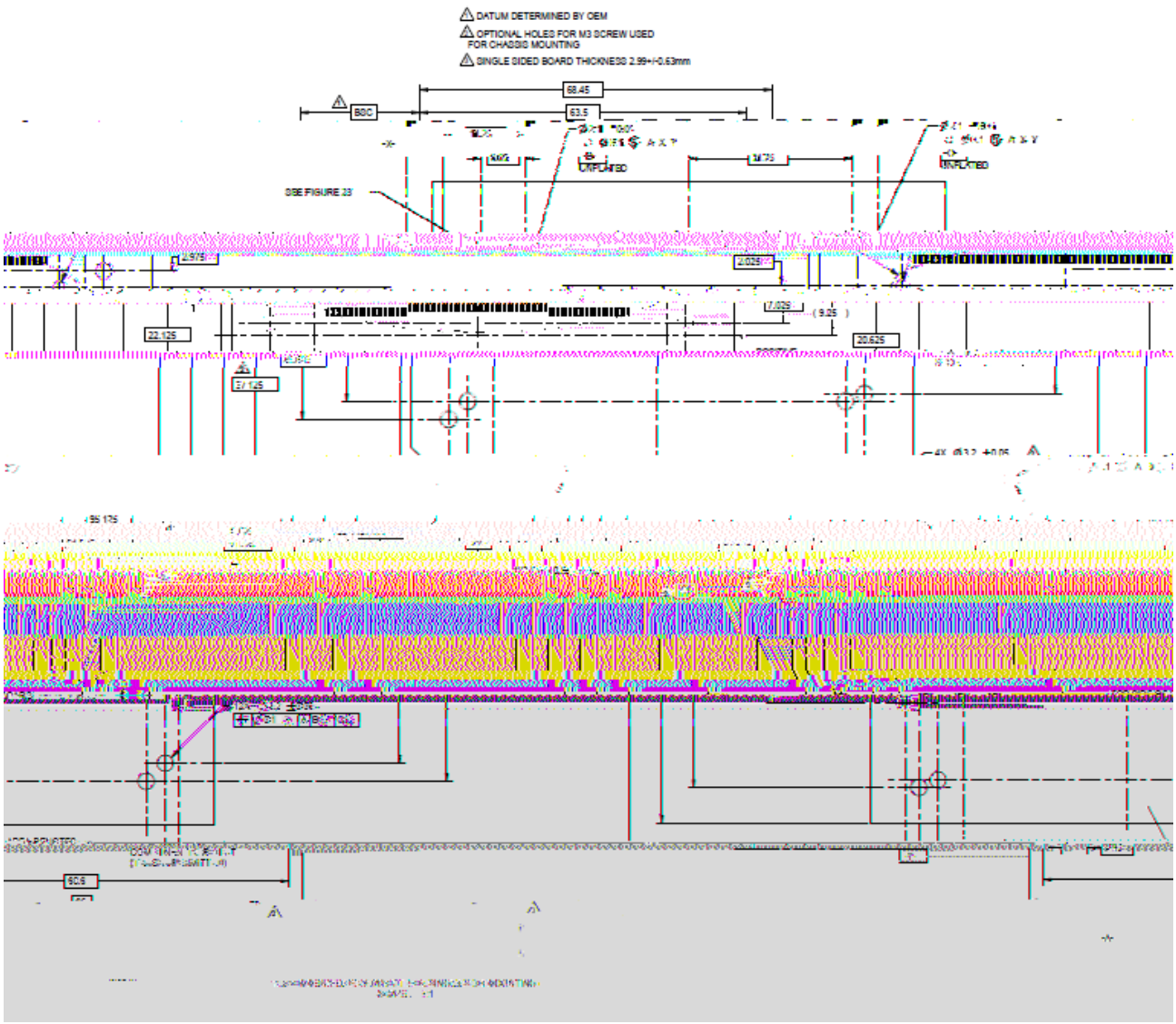
50	VND_IO_F	I/O		Module Vendor I/O F. Do Not Connect
51	VND_IO_G	I/O		Module Vendor I/O G. Do Not Connect
52	GND			
53	VND_IO_H	I/O		Module Vendor I/O H. Do Not Connect
54	VND_IO_J	I/O		Module Vendor I/O J. Do Not Connect
55	3.3V_GND			3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal
56	3.3V_GND			
57	3.3V_GND			
58	3.3V_GND			
59	3.3V_GND			
60	3.3V			3.3V Module Supply Votage
61	3.3V			
62	3.3V			

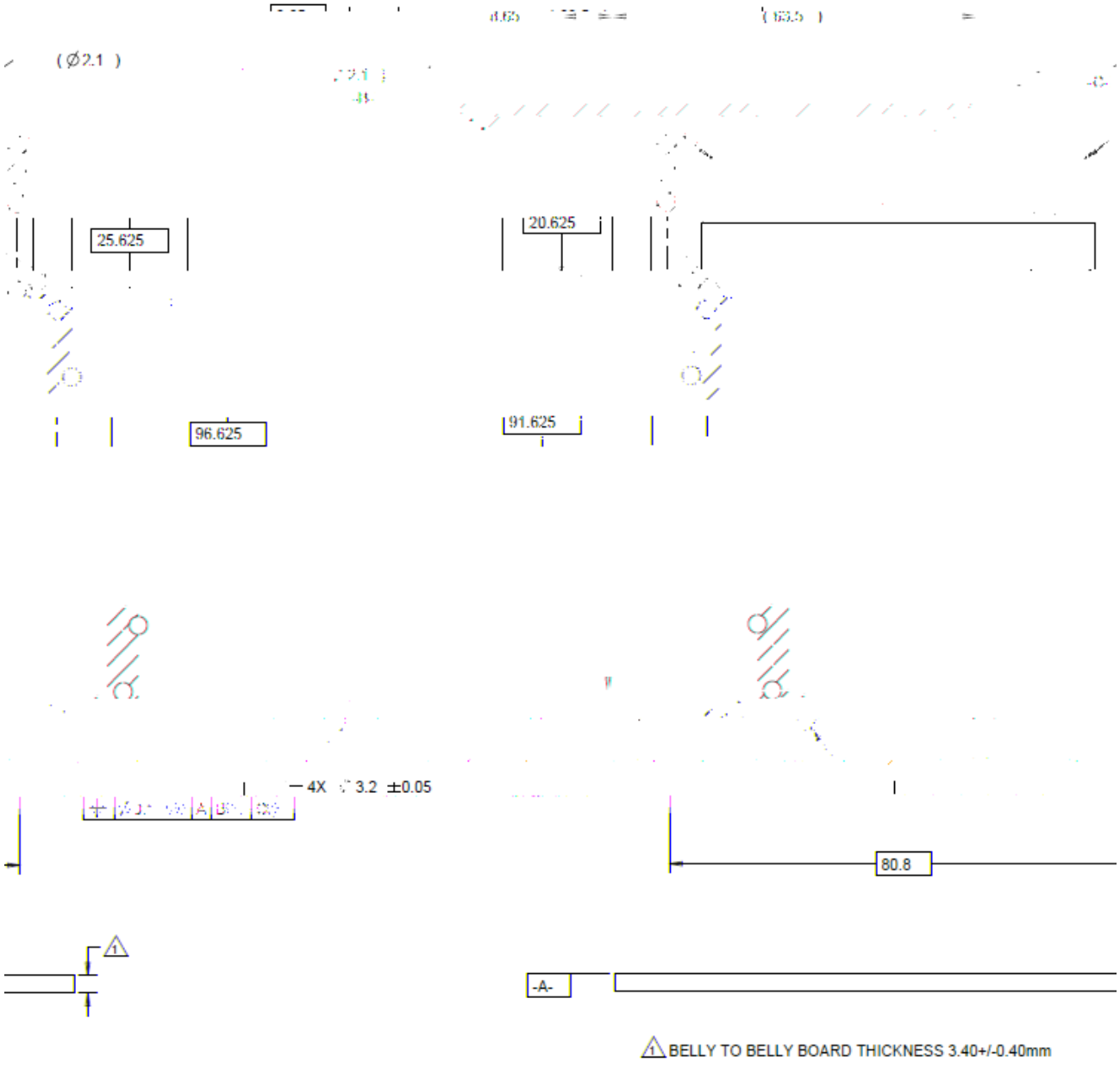
89	RX3n	O	CML	Inverted Output Data
90	GND			
91	RX4p	O	CML	Output Data
92	RX4n	O	CML	Inverted Output Data
93	GND			
94	RX5p	O	CML	Output Data
95	RX5n	O	CML	Inverted Output Data
96				

130	GND			
131	TX6p	In	CML	Input Data
132	TX6n	In	CML	Inverted Input Data
133	GND			
134	TX7p	In	CML	Input Data
135	TX7n	In	CML	Inverted Input Data
136	GND			
137	TX8p	In	CML	Input Data
138	TX8n	In	CML	Inverted Input Data
139	GND			
140	TX9p	In	CML	Input Data
141	TX9n	In	CML	Inverted Input Data
142	GND			
143	N.C.			
144	N.C.			
145	GND			

Block diagram

Package outline


DATUM DETERMINED BY OEM
OPTIONAL HOLES FOR M3 SCREW USED FOR CHASSIS MOUNTING
SINGLE SIDED BOARD THICKNESS 2.99+/-0.63mm
68.45
63.5
SEE FIGURE 33
22.125
20.625



1 BELLY TO BELLY BOARD THICKNESS 3.40+/-0.40mm

FIGURE 21

Regulatory Compliance

Feature	Test Method	Performance
Electrostatic Discharge (ESD) to the Electrical Pins	MIL-STD-883E Method 3015.7	

	CENELEC EN55022 VCCI Class 1	
Immunity	IEC61000-4-3 Class 2	Compliant with any electo-