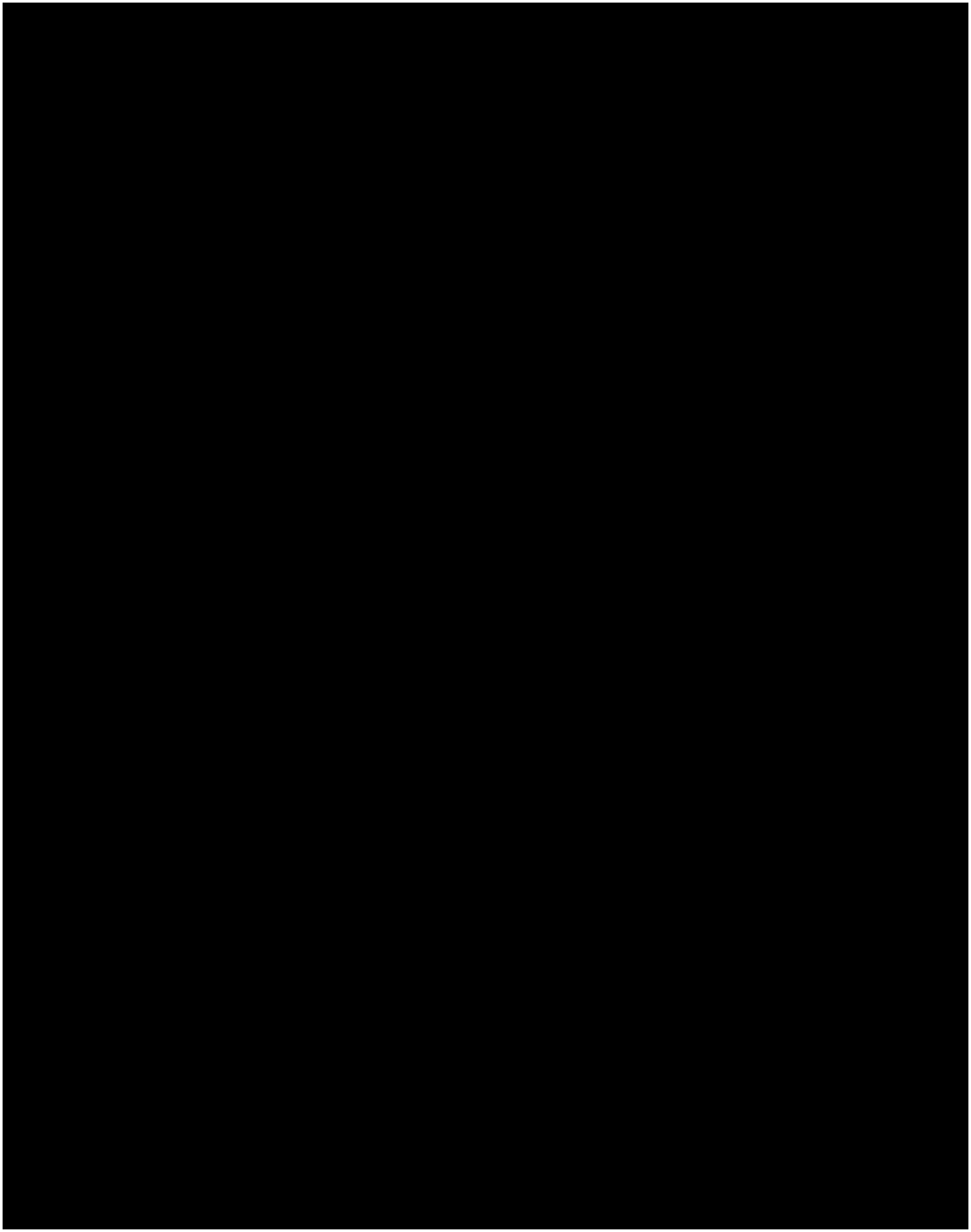
100Gb/s CFP Optical Transceiver



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Note1.

Note2.

Note4.
Note5.

Note6.

Note7.

Note8.
Note9.

Note10.
Note11.

Hardware Control Pins

Note2:

Hardware Alarm Pins

		RO/LH/COR				
		RO/LH/COR				
		RO/LH/COR				
		RO/LH/COR				

				Module General Status Enable		

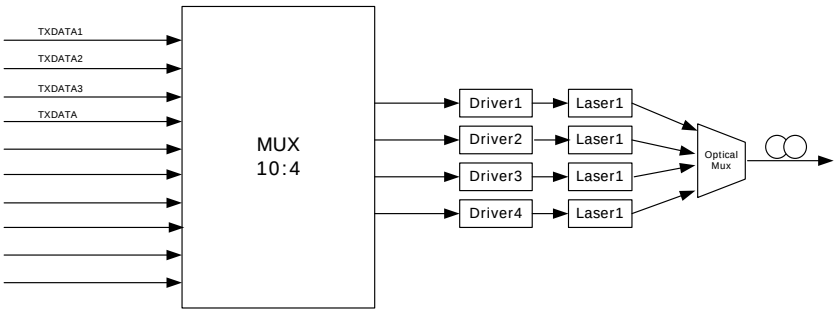
Network Lane FAWS Latch Registers						
				Network Lane n Alarm and Warning Latch		

Table : CFP Pin-Map

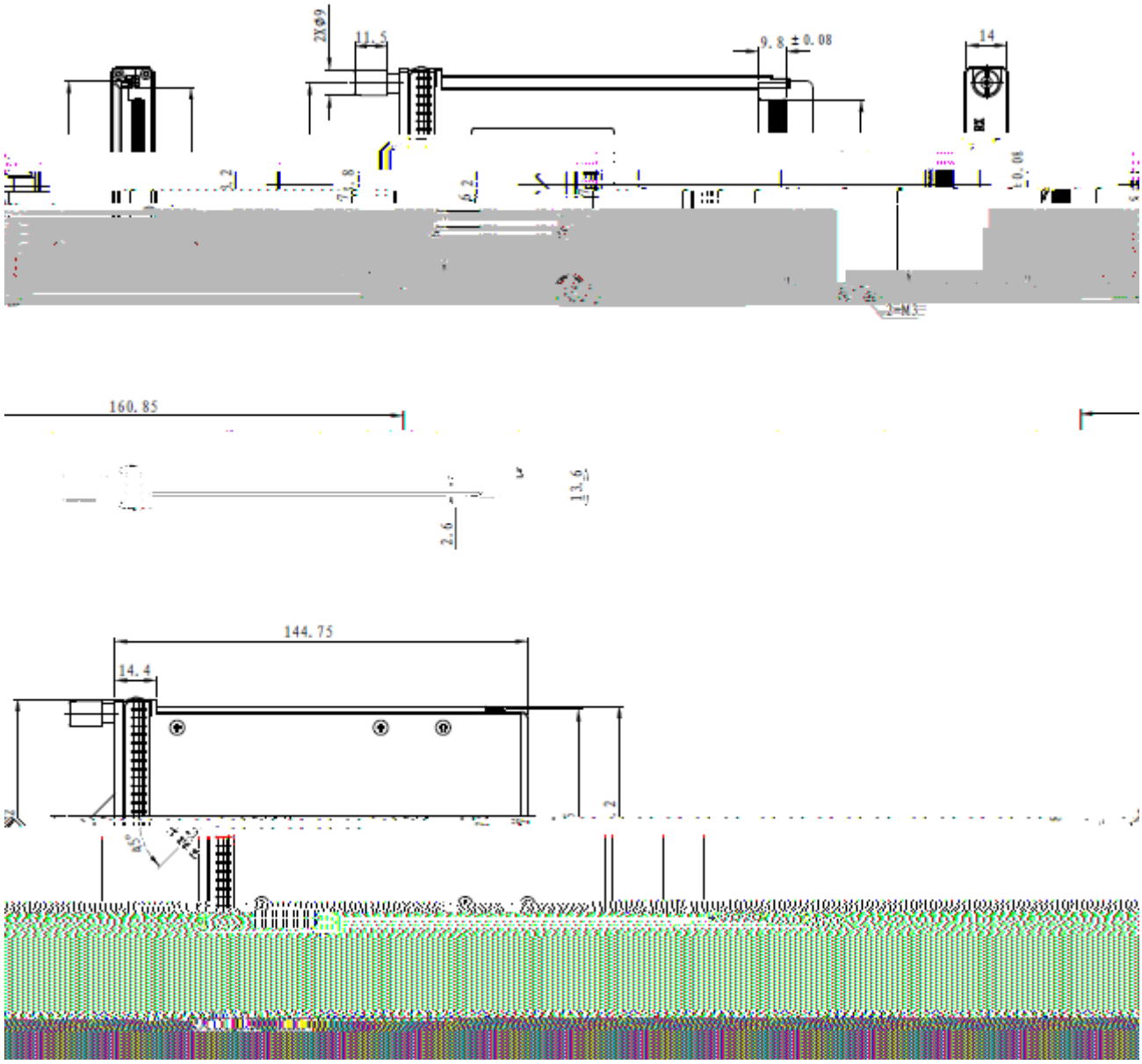
PIN#	Top Row (2nd Half) Name	PIN#	Bottom Row (2nd Half) Name	PIN#	Top Row (1nd Half) Name	PIN#	Bottom Row (1nd Half) Name

				" " " "
				" " " "

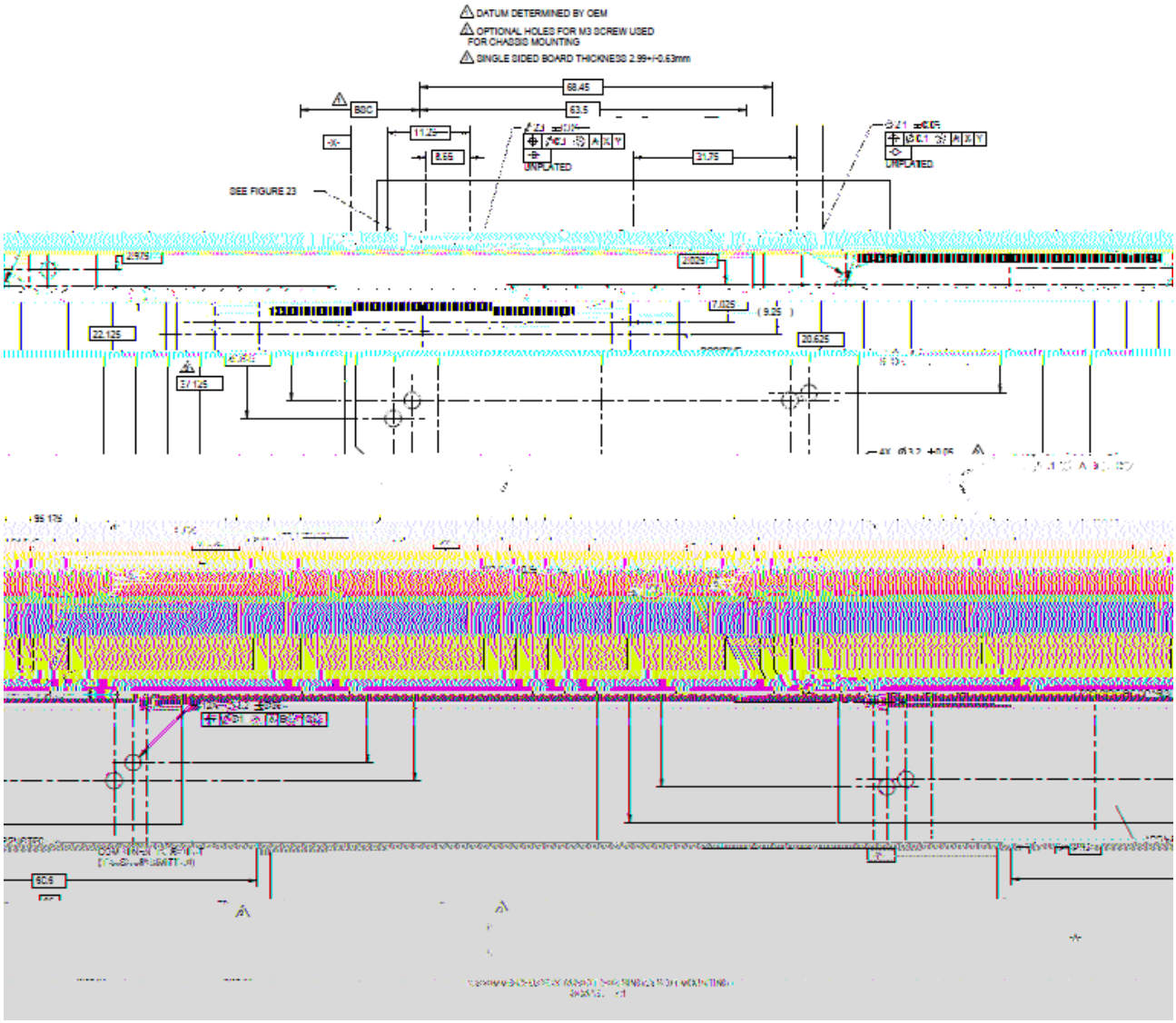
Block diagram

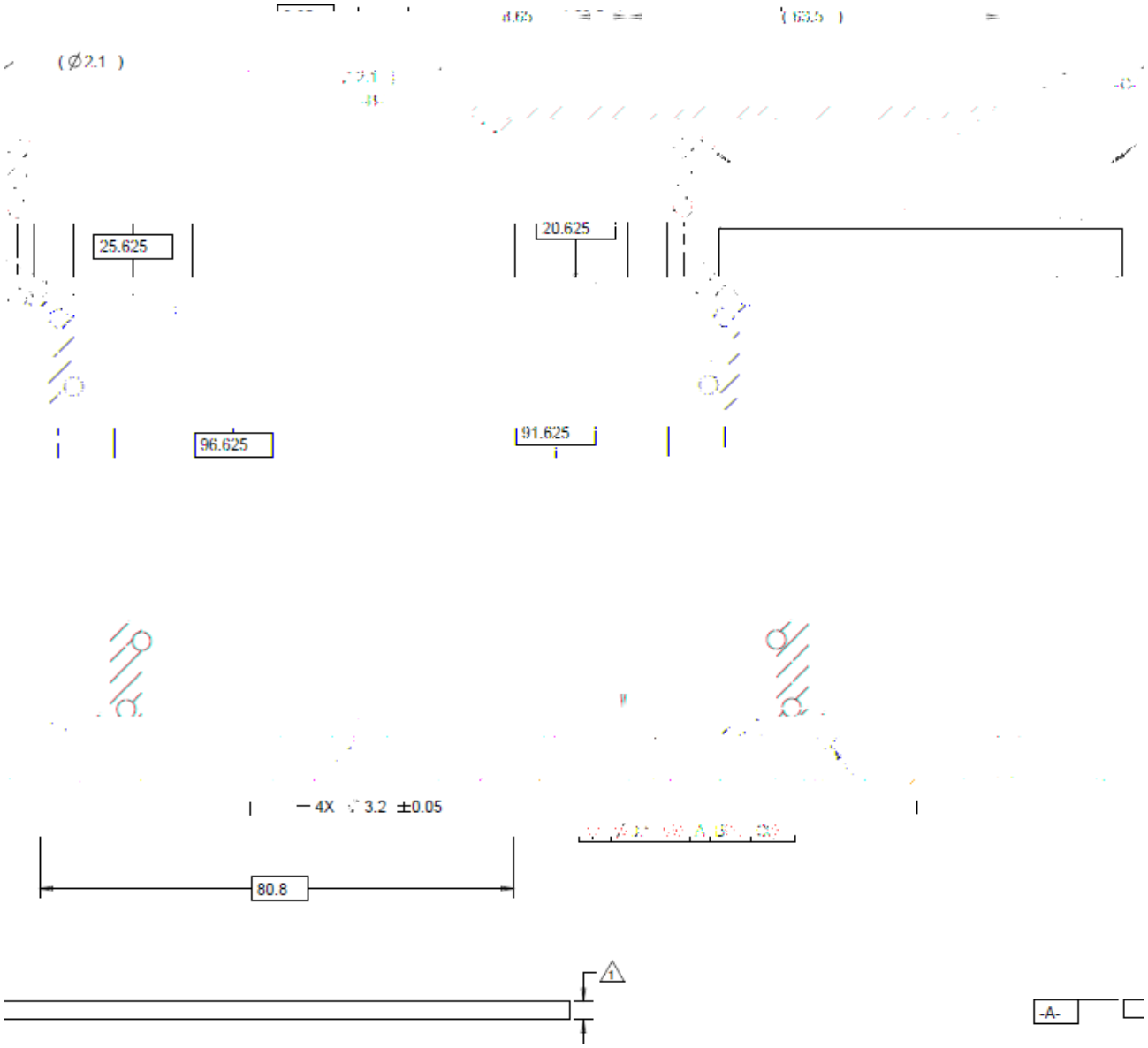


Package outline



PCB layout recommendation





1 BELLY TO BELLY BOARD THICKNESS 3.40+/-0.40mm

FIGURE 21

Regulatory Compliance

Feature	Test Method	Performance